33. (Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

C1

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, the data and common electrodes having portions for first and second storage capacitors;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlapping the gate and data bus lines; and

a first alignment layer on the common electrode.

48. (Amended) An in-plane switching mode liquid crystal display comprising:

C2

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region, wherein the common electrode has first and second oblique sides;

a passivation layer over the thin film transistor and the data electrode; and

a first alignment layer on the common electrode.

64. (Amended) An in-plane switching mode liquid crystal display comprising:

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

C3

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode;

a light shielding layer on the passivation layer; and

a first alignment layer on the common electrode.

69. (Amended) An in-plane switching mode liquid crystal display comprising:

C4

gate and data bus lines on a first substrate defining a pixel region;

a common bus line parallel to the gate bus line;

a thin film transistor at a crossing of the gate and data bus lines, the thin film transistor having a gate electrode, a gate insulator, a semiconductor layer, a source electrode, and a drain electrode;

data and common electrodes parallel to the data bus line in the pixel region;

a passivation layer over the thin film transistor and the data electrode, wherein the common electrode is formed on the passivation layer parallel to the data electrode and overlaps the gate and data bus lines;

a light shielding layer on the passivation layer; and

a first alignment layer on the common electrode.